IN THE CLAIMS

No amendments to the claims are requested. The currently-pending claims are:

1. (Original) A system comprising:
a processor coupled to a bus;
a memory coupled to the bus;
an external bus controller coupled to the bus; and
a basic input-output system (BIOS) coupled to the bus, the BIOS comprising an external bus support component to cause a periodic interrupt to be generated and to provide support for external bus enabled devices responsive to the periodic interrupt.

2. (Original) The system of claim 1 wherein the external bus support component is to provide support for external bus enabled devices until an operating system providing external bus support is loaded.

3. (Original) The system of claim 1 wherein the external bus enabled devices comprise at least one of a keyboard, a mouse, a floppy drive, a biometric device, a hard disk drive, a compact disk read-only memory (CD-ROM) player.

4. (Original) The system of claim 1 wherein:
the external bus controller is a Universal Serial Bus (USB) host controller;
the external bus support component is a USB support component; and
the external bus enabled devices are USB devices.

5. (Original) The system of claim 1 wherein the memory is mapped according to the Advanced Configuration and Power Interface (ACPI) specification and the BIOS comprises a software component to implement the ACPI specification.

6. (Original) The system of claim 1 wherein the processor conforms to the 32 bit Intel Architecture (IA-32) and the periodic interrupt is a system management interrupt (SMI).

7. (Original) The system of claim 1 wherein the processor is compatible with the 32 bit Intel Architecture (IA-32).

8. (Original) A system comprising:

a processor coupled to a bus;

a memory coupled to the bus;

an external bus controller coupled to the bus;

an external bus enabled device coupled to the external bus controller;

a basic input-output system (BIOS) coupled to the bus, the BIOS having instructions which when executed cause the processor to perform operations comprising:

obtaining a portion of the memory to be used to maintain a plurality of external bus device data;

causing an interrupt to be periodically generated; and

handling input produced by the external bus enabled device using the portion of the memory responsive to the interrupt.

9. (Original) The system of claim 8 wherein the processor conforms to the 32-bit Intel Architecture (IA-32) and the interrupt is a system management interrupt (SMI).

10. (Original) The system of claim 8 wherein the BIOS has further instructions which when executed cause the processor to perform further operations comprising:

disabling the periodically generated interrupt when an operating system providing external bus device support is completely loaded.

11. (Original) The system of claim 8 wherein the BIOS has further instructions which when executed cause the processor to perform further operations comprising:

de-allocating the portion of the memory when an operating system providing external bus device support is completely loaded.

12. (Original) The system of claim 8 wherein:
the external bus controller is a Universal Serial Bus (USB) host controller;
the external bus support component is a USB support component; and
the external bus enabled device is a USB device.

13. (Original) The system of claim 8 wherein obtaining comprises:
mapping a memory pursuant to the Advanced Configuration and Power Interface (ACPI) specification to include a non-volatile-sleeping (NVS) memory region such that the portion of the memory is in the NVS memory region.

14. (Previously Presented) A method comprising:
obtaining a portion of a memory to be used to maintain a plurality of USB device data;
causing an interrupt to be periodically generated by an external bus support component; and
handling input produced by one or more USB devices using the portion of the memory.

15. (Original) The method of claim 14 wherein the interrupt is a system management interrupt (SMI) of the 32-bit Intel Architecture (IA-32).

16. (Original) The method of claim 14 further comprising:
disabling the periodically generated interrupt when an operating system providing USB device support is completely loaded.

17. (Original) The method of claim 14 further comprising:
de-allocating the portion of the memory when an operating system providing USB device support is completely loaded.

18. (Original) The method of claim 14 further comprising:

mapping a memory pursuant to the Advanced Configuration and Power Interface (ACPI) specification to include a non-volatile-sleeping (NVS) memory region such that the portion of the memory is in the NVS memory region.

19. (Original) The method of claim 14 further comprising:

sending data to one or more USB devices using the portion of the memory.

20. (Original) The method of claim 14 further comprising:

determining whether an operating system providing USB device support is loaded.

21. (Original) The method of claim 20 wherein determining comprises:

checking a frame list base address register value to determine whether it is set to the address of the portion of the memory.

22. (Original) The method of claim 14 further comprising:

disabling conversion of USB hardware interrupts into USB legacy software interrupts; and

disabling the hardware generated USB interrupts.

23. (Original) The method of claim 14 further comprising:

adjusting the rate of the interrupt based on data traffic involving the one or more USB devices.

24. (Original) A machine readable medium having instructions thereon which when executed by a processor cause the instructions to be copied to a basic input-output system (BIOS) such that during subsequent boot up of a system including the processor, the processor performs operations comprising:

obtaining a portion of a memory to be used to maintain a plurality of external bus device data;

causing an interrupt to be periodically generated; and

handling input produced by an external bus enabled device using the portion of the memory responsive to the interrupt.

25. (Original) The machine readable medium of claim 24 wherein the processor conforms to the 32-bit Intel Architecture (IA-32) and the interrupt is a system management interrupt (SMI).

26. (Original) The machine readable medium of claim 24 having further instructions thereon which, after being copied to the BIOS, when executed, cause the processor to perform further operations comprising:

disabling the periodically generated interrupt when an operating system providing external bus device support is completely loaded.

27. (Original) The machine readable medium of claim 24 having further instructions thereon which, after being copied to the BIOS, when executed, cause the processor to perform further operations comprising:

de-allocating the portion of the memory when an operating system providing external bus device support is completely loaded.

28. (Original) The system of claim 24 wherein:

the external bus controller is a Universal Serial Bus (USB) host controller;

the external bus support component is a USB support component; and

the external bus enabled device is a USB device.

29. (Original) The machine readable medium of claim 24 wherein obtaining comprises:

mapping the memory pursuant to the Advanced Configuration and Power Interface (ACPI) specification to include a non-volatile-sleeping (NVS) memory region such that the portion of the memory is in the NVS memory region.